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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,940	11/21/2000	Shiro Sakiyama	10873.589USW	4531

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EXAMINER	
EVERHART, CARIDAD	
ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,940	SAKIYAMA ET AL.	
	Examiner	Art Unit	
	Caridad M. Everhart	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant has argued that Miki teaches determining a wiring capacitance value after the arranging by a layout method. This argument is respectfully not considered persuasive because the rejection in made in view of the combined references. Miki is relied upon only for the method of determining the value of the capacitance. Applicant has further argued that neither Miki nor Hulse teach an automatic layout method. Hulse teaches a method in which the value is determined before the layout step, as Hulse teaches simulation using a simulation tool for the layout method(col. 5,lines 54-63), which would be carried out in order to determine the layout, as Husle teaches that the simulation is carried out "before ...it is commited to silicon". That the method is automatic is disclosed by that the simulation tool carries out the design(col. 5, lines 54-63) and that the layout is carried out automatically by algorithm (col. 3,lines 31-25) .

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1,2, 4, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hulse, et al. (US 6,618,847B1) in view of Miki (US 5,761,076).. Hulse, et al disclose placing capacitor cells around the logic cells(abstract and col. 1,lines 58-60). The layout is automatically calculated by algorithm(3, lines 31-35). It is

clear that the layout for the logic cells is determined , and then the capacitor cells are placed(col. 5, lines 7-10). The capacitor cells are also coupled to the power and ground(claim 17, and col. 4,lines 58-65, in which the "filler cells" are the capacitor cells).

Hulse, et al is silent with respect to the method of calculation of the capacitance.

Miki discloses the determination of the capacitance by using the logic gates(col. 1, lines 20-32 and col. 2, lines 33-37). These calculations are done in the determination of the layout (col. 4, lines 1-5,12-15, and 25-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have determined the capacitance using the logic gates in the layout method disclosed by Hulse, et al as taught by Miki because Miki discloses that these calculations are an improvement in the computer design of layout of logic gates and capacitance(col. 1, lines 15-19and 53-60). With respect to the value recited in claim 2, one of ordinary skill in the art would be able to determine the safety margin which would be desired in the design of the cells in the value of the capacitance.

Claims 1,2, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita (US 5,869,852) in view of Miki (US 5,761,076). Kinoshita discloses a method for layout of logic cells (col. 1, lines 10-15 and 36-40) and capacitors in cells between the logic cells and the power supply (col. 1,lines 42-46 and col. 2, lines 50-55 and col. 15, lines 1-11). The capacitor cells are in the vicinity of the logic cells(col. 2, lines 65-68, and col. 3, lines 1-3). Because Kinoshita teaches that the capacitor cells are between the logic cells (col. 4, lines 57-65), this is interpreted as that

the cells are in areas where the logic cells are not arranged, as required by claim 4. The arrangement is carried out by computer(col. 6, lines 53-59), so that the method is an automatic method. Although Kinoshita discloses logic cells rather than logic gate cells, logic cells are the same because logic cells would be made up of logic gates. The number of capacitor cells is calculated based on the available space between the logic cells (col. 4, lines 57-65), as the disclosure of the dimensions of the capacitor cells being taken into account and the arranging of the cells in the spaces between the logic cells would involve the calculation of how many cells of these dimensions could be placed in the space.

Kinoshita is silent with respect to the logic gate cell being used to determine the capacitance value.

Miki discloses the determination of the capacitance by using the logic gates(col. 1, lines 20-32 and col. 2, lines 33-37). These calculations are done in the determination of the layout (col. 4, lines 1-5,12-15, and 25-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have determined the capacitance using the logic gates in the layout method disclosed by Kinoshita as taught by Miki because Miki discloses that these calculations are an improvement in the computer design of layout of logic gates and capacitance(col. 1, lines 15-19and 53-60). With respect to the value recited in claim 2, one of ordinary skill in the art would be able to determine the safety margin which would be desired in the design of the cells in the value of the capacitance.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita in view of Miki as applied to claim1 above, and further in view of Kusunoki, et al (US 5,512,766).

Kinoshita in view of Miki is silent with respect to the details of the power supply capacitance cell.

Kusunoki is relied upon for its teaching of the details of a unit capacitor cell which includes the n region and the polycrystalline silicon layer connected to the voltage source (col. 9, lines 49-64 snf vol. 10, lines 40-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Kusunoki with the device and method taught by Kinoshita in view of Miki because the capacitor cell taught by Kusunoki can be made to provide the capacitance required for a capacitor from a voltage source to logic block cells (Kusunoki, col. 3, lines 22-33).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunoshita in view of Miki as applied to claim1 above, and further in view of Eto, et al. (US 6,229,363B1).

Kunoshita in view of Miki is silent with respect to clock synchronization.
Eto et al disclose tat clock signals are required for the functioning of logic cells (col. 1, lines 44-48; col. 3, lines 22-26 and col. 5, lines 61-67).

It would have been obvious to one of ordinary skill in the art to have combined clock synchronization elements with the device taught by Kunoshita in view of Miki

because Eto et al disclose that it is known in the prior art to us clock synchronization with logic and capacitance elements.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caridad M. Everhart whose telephone number is 571-272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, B. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Everhart

CARIDAD EVERHART
PRIMARY EXAMINER

C. Everhart
1-2-2006